SYSTEM AND METHOD FOR ENHANCING THE SPEED OF DYNAMIC TIMING SIMULATION USING DELAY ASSESSMENT AT COMPILE TIME

ABSTRACT OF THE DISCLOSURE

A method and system for reducing the time required for execution of the dynamic timing simulation for a logic simulator. For a logic circuit simulator having a compilation phase and a runtime phase, a delay assessment is performed during the compilation phase in order to identify storage elements that are exempt from possible timing violations at runtime. The runtime timing checks are removed from the exempt storage elements, thereby reducing the runtime calculation effort. Additionally, combinational portions of the circuit that drive the exempt storage elements are examined for element delays that can be effectively eliminated (e.g., zero delayed) from the runtime calculations, thereby providing a further reduction in the computational overhead via the use of cycle based simulation for these.